PREDECODE COLUMN ARCHITECTURE AND METHOD

ABSTRACT OF THE DISCLOSURE

A system and method for predecoding memory addresses by generating a sequence of predecode signals based on the memory address, providing the sequence of predecode signals as a first set of activation signals, and based on the value of the memory address, either resequencing the sequence of predecode signals and providing the resequenced predecode signals as a second set of activation signals or providing the sequence of predecode signals as the second set of activation signals.

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